Department of Electronics and Communication Engineering

Ref. RVITM/ECE/ /2024-25

Date: 26.11.2024

Title of Program:	**Verilog in Semiconductor Industry-Future Scope**
Type of the Program (SDP/FDP/Talk/Workshop/etc.)	INDUSTRY EXPERT TECHNICAL TALK
Date & Time of the Proposed Program:	26-11-2024 from 02:00 PM to 03:15 PM
Department:	ELECTRONICS & COMMUNICATION ENGINEERING
Nature of Program:	Student Knowledge Enhancement Programme in Digital System Design using Verilog course
Objectives of the Program:	To prepare students for the industry in the field of Electronics (VLSI).
Proposal submitted by (Name) :	Prof. PRASHANT P PATAVARDHAN
Target Audience & Number:	3RD SEMESTER and 70 Students
Outcome of Programme:	The students will be able to gain the information about the Core Electronics/Semiconductor Industry requirements.
POs to be addressed:	PO2, PO3, PO4, PO5, and PO12
Can the Program be linked to any of the curriculum subject? If so which subjects?	YES DIGITAL SYSTEM DESIGN USING VERILOG (BEC302) [IPCC]
Benefit to the Students :	Students will be strongly familiarized with the hardware design, enhance problem solving skills and exposure to simulation tools.
Benefit to the Faculties :	Shall ✓ Enhance research opportunities, ✓ Prepare for industry collaboration, and ✓ Staying connected with current trends.
Benefit to the Institute (MOU, Consultancy, Projects, Funding, Placements, etc:)	▪ Strengthen Industry Connections, ▪ Enhance Learning Environment, and ▪ Curriculum Improvement.
Resourse Person (Attach Profile of the Resource Person)	Mrs. ROOPA K SWAMY Senior Engineer, Design Verification INNOPHASE IOT SOLUTIONS, BANGALORE
Programme Convener/HOD:	Dr. Manjunatha Prasad R, VP & HOD-ECE
Programme Coordinator:	Prof. PRASHANT P PATAVARDHAN

Executive Summary of the Event:

The technical talk began with a welcome speech by Mr. Adyot, a 3rd-semester ECE student. He introduced the resource person, Mrs. Roopa K. Swamy, Senior Engineer, DV, Innophase IoT, Bengaluru.

The talk on "Verilog in Semiconductor Industry-Future Scope" which delves into the critical role of Verilog, a hardware description language (HDL), in the design and development of semiconductor systems. Verilog has become an essential tool for designing digital circuits, and its importance continues to grow in the ever-evolving semiconductor industry. The session explored the current applications of Verilog, its influence on semiconductor technology, and the future trends that are shaping the industry. By examining advancements in Verilog and its integration with emerging technologies, the talk highlighted the increasing demand for skilled professionals proficient in Verilog, as well as the expanding career opportunities in semiconductor design.

The future scope of the semiconductor industry in India is closely tied to innovations in 5G infrastructure, AI-driven chips, and IoT devices. As semiconductor designs become more complex, there will be a growing demand for engineers proficient in Verilog and System Verilog. Career opportunities in areas like digital circuit design, verification engineering, embedded systems, and product development are abundant.

To be industry-ready, aspiring professionals must master key concepts such as Verilog and System Verilog, digital logic design, simulation tools, FPGA programming, and an understanding of semiconductor manufacturing processes. Staying updated with emerging technologies and industry trends will be crucial for success in this rapidly evolving field.

The Vice-Principal and HOD of ECE highlighted the importance of such industry expert talks in bridging the gap to the core electronics industry. The Vice-Principal also appreciated the efforts put in by the resource person. The session was concluded with a vote of thanks delivered by Mr. Adyot.

The technical talk was organized in association with RVITM IETE ISF.
(THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS STUDENT FORUM)

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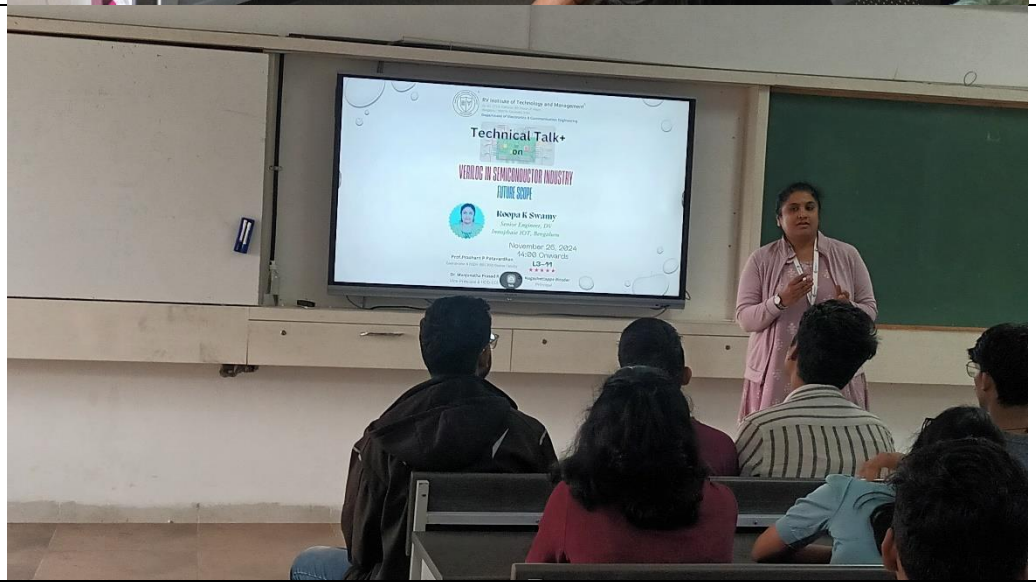

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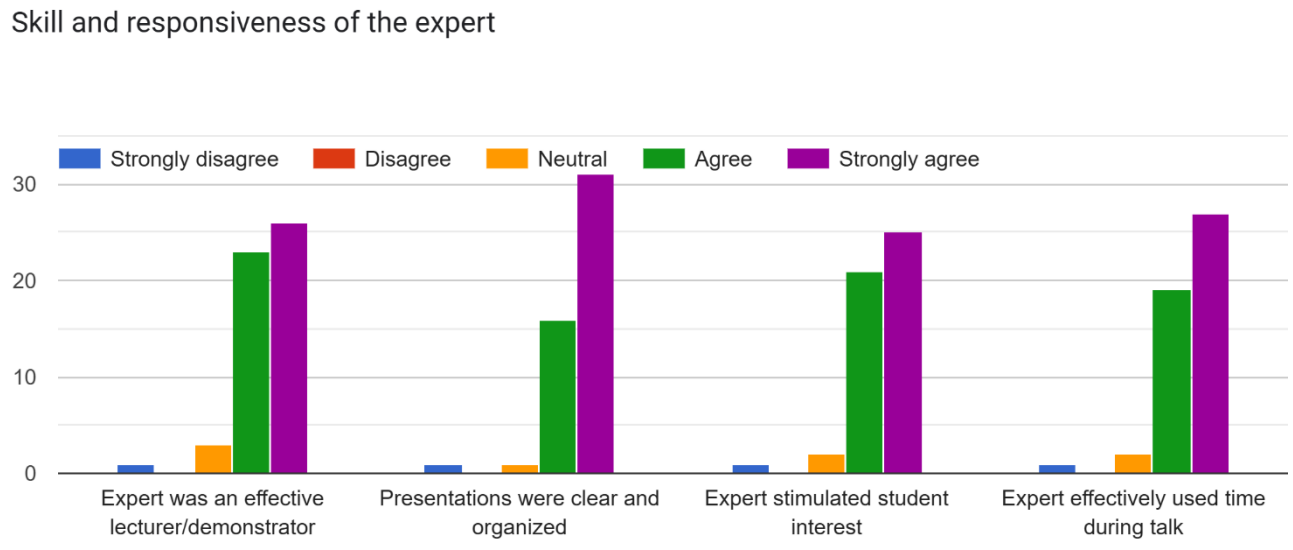
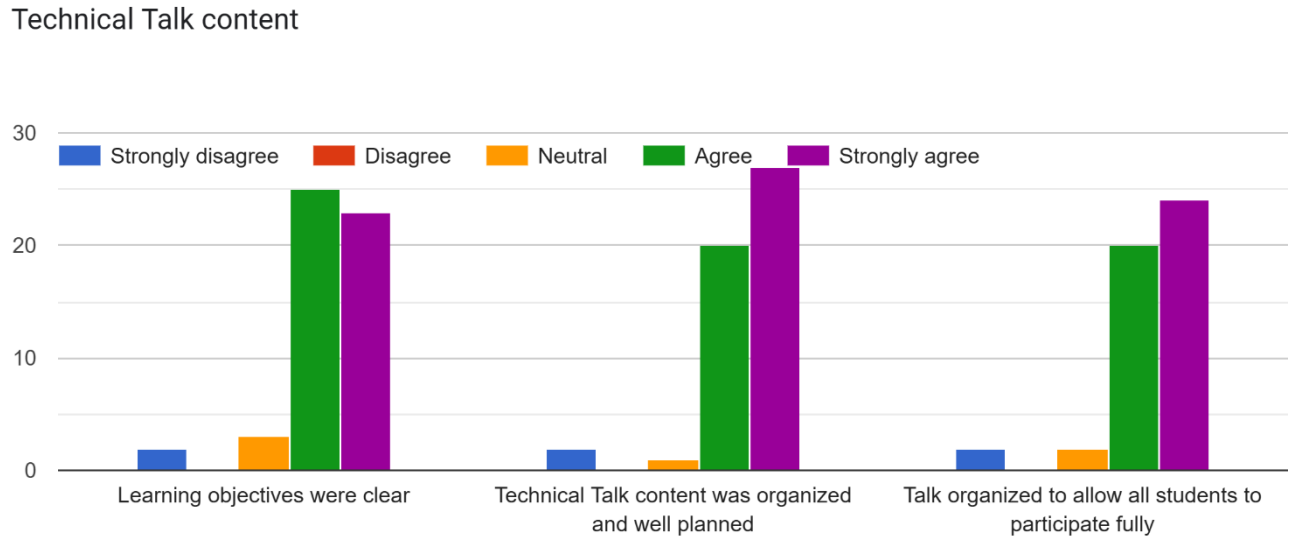
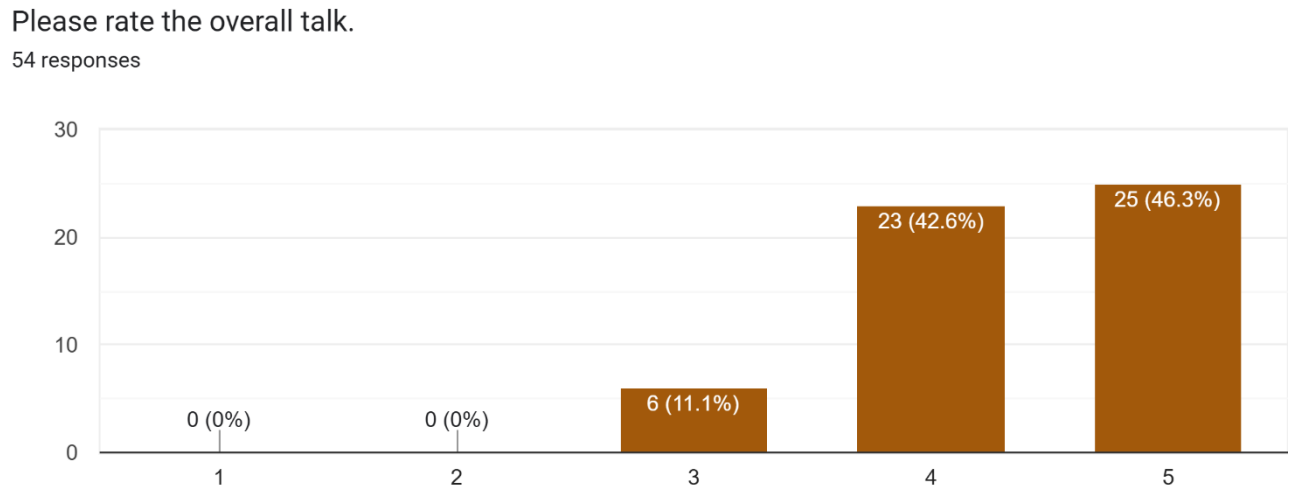
Students feedback:







Key Learning outcomes based on students understanding:
Future of semiconductor
Opportunity in semiconductor
Job role
Industry application of Verilog

Resource Person Profile:

Roopa K Swamy is currently working at Senior Engineer, DV at Innophase IOT, Bangalore since February 2023. She is involved in bringing up Design Verification-UVM environment at SoC level verification, UVM RAL setup and GLS setup and verification. Worked on 3 critical tapeouts. Expertized in UVM, SV, GLS verification and debug.

Always been an adaptive, hardworking, and Curious learner

Roopa K Swamy holds a Bachelor of Engineering in Electronics and Communication Engineering from MCE, Hassan and MTech in VLSI Design Embedded System from SJCE, Mysore in the year 2012.

She has an experience of working in verification domain at LSI India Pvt. Ltd. for an year. She then worked as Assistant Profession at SJBIT for 7 years and joined CoreEL Technologies India Pvt. Ltd. worked as Faculty – Sandeepani for 3 years from February 2020 to February 2023.

At CoreEL Technologies she is involved in delivering training for corporate professional and students. She has trained Customers at various government and private organizations like IRDE, DRDO, DLJ-Jodhpur, NTIS-Saudi, Lekhawireless, VVDN Technologies.

Delivered trainings on different technologies and tools:

- Programming Languages –Verilog, VHDL, SV
- Verification Methodology- UVM
- FPGA Design flow using Xilinx Vivado Design Suite
- UltraFast Design Methodology
- Static Timing Analysis
- FPGA technologies – 7 series architecture, Zynq SoC
- EDA Packages – Xilinx Vivado, Mentor Graphics QuestaSim
- Cadence - Xcelium, Vmanager, Agnisys