Professional summary

Over **4.5 years of combined experience** in industry and academia, with specialization in **VLSI design and verification**. Strong proficiency in industry-standard tools and methodologies, with effective integration of practical industry exposure into teaching and academic activities. Actively involved in teaching, research, and academic development, with a commitment to continuous learning and quality academic outcomes.

Skills

CMOS behavior
Digital Logic design
ASIC design flow
Static Timing Analysis (STA)
Bluetooth Layers
Physical design methodology
Teaching
Synopsys VCS tool
Cadence Virtuoso
Xilinx

Websites, Portfolios, Profiles

www.linkedin.com/in/nivedita-s-desai

Work history

Assistant Professor [ECE Dept] RV Institute of Technology and Management Bengaluru, India

Demonstrated strong expertise in delivering engaging and effective lectures across core Electronics and Communication Engineering subjects.
Implemented innovative pedagogical approaches, including flipped classrooms, project-based learning, and interactive teaching methods, to enhance student engagement and academic outcomes.
Actively guided and connected students with relevant hackathons and internship opportunities to promote hands-on industry exposure.
Authored the textbook *"VLSI Design and Technology"* as the first author, designed for Electronics and Communication Engineering students.
Granted five patents, including four international patents and one Indian patent; additionally, two Indian patents have been filed and are currently under examination.
Awarded one international copyright grant from Canada.
Published research as an author in one Q1 journal, two Q4 journals, and one international conference proceeding.

Snr. Software Engineer LTI Mindtree

Jan 2022 to May 2024

Utilized industry-standard EDA tools, such as VCS, on the Linux platform to simulate and analyze VLSI designs, ensuring compliance with design rules and specifications.

Currently, I am looking into the understanding of MODEM, multiple blocks inside the MODEM, and bringing in design modifications using Verilog HDL.
Understand and analyze the RTL code of different blocks in the controller.
Development and testing of Bluetooth transmission reception mode, along with audio testing using an FPGA-MPS2 board.
Developed the test cases based on the available requirement specifications and verification plans.
Creating and maintaining regression test suites. Debugged multiple regression failures.
Capable of working both as an independent contributor and a team member.

Academic Intern at Mindtree Pvt Ltd

Oct 2020 to aug 2021
Good knowledge of Bluetooth working, modes of operation, and PCM-IIS CODEC interface.
Developed test cases using base test cases for PCM audio conversion scenarios, and similarly for IIS, based on data format using different registers according to their functionality.
Understood the AHB protocol and used the signals to observe data packet transmission and reception. Exposed to the usage of the Linux platform.
Strong understanding of the RTL2GDSII flow for leading or mainstream process technologies.
Good understanding of the concepts related to synthesis, place and route, and CTS.

Education

MTech from RV College of Engineering in VLSI and Embedded systems graduated in august 2021.

Pursued masters in VLSI and Embedded systems with a CGPA of 8.47 under VTU.
Bachelors of Engineering from Jyothy Institute of Technology in Electronics and Communication Engineering and graduated in May 2019.
Pursued Electronics and Communications with a CGPA of 6.25 under VTU.

Accomplishments

1. Secured **6th position** as a team member in the **GreenMind Sustainable AI Hackathon**, held on **31 October 2025** at Sir M. Visvesvaraya Institute of Technology, Yelahanka, Bengaluru, Karnataka, India.
2. Recognized as 4th **Finalist in the Systems Software Track** at the **DIR- V Symposium 2025 Hackathon** held on **2nd and 3rd March 2025 at** IITM Research Park, Chennai , in acknowledgment of outstanding performance and technical contribution.

FDPs Attended

1. Successfully participated in and completed the **AICTE–ATAL Academy Faculty Development Program** titled *“Innovative VLSI Paradigms: MEMS,*

3D ICs, and AI-Driven Design”, conducted at **Vidya Vikas Institute of Engineering & Technology**, from **06 January 2025 to 11 January 2025**.
2. Successfully participated in and completed the **Faculty Development Program on “AI-Driven Image Intelligence: Advances in Processing and Learning”**, conducted by the **Electronics and ICT Academy, IIT Guwahati**, from **08 September 2025 to 12 September 2025**, securing a **B grade with a score of 70/100**.

Languages

- **Verilog**
- **Basics of SV**
- **C**

Certifications

Jan 2025 - Successfully participated in and completed the AICTE–ATAL Academy Faculty Development Program titled “Innovative VLSI Paradigms: MEMS, 3D ICs, and AI-Driven Design”, conducted at Vidya Vikas Institute of Engineering & Technology, from 06 January 2025 to 11 January 2025.

Sep 2025- Successfully participated in and completed the Faculty Development Program on “AI-Driven Image Intelligence: Advances in Processing and Learning”, conducted by the Electronics and ICT Academy, IIT Guwahati, from 08 September 2025 to 12 September 2025, securing a B grade with a score of 70/100.